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APPLICANTS	:	Thomas D. FLETCHER
SERIAL NO.	:	09/956,903
FILED	:	September 21, 2001
FOR	:	SYMMETRIC CASCADED DOMINO CARRY GENERATE GATE
GROUP ART UNIT	:	2193
EXAMINER	:	Chat C. DO

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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 950.00

Complete if Known	
Application Number	09/956,903
Filing Date	September 21, 2001
First Named Inventor	Thomas D. FLETCHER
Examiner Name	Chat C. DO
Art Unit	2193
Attorney Docket No.	Intel 2207/11270

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2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

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1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
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1252	450	2252	225	Extension for reply within second month	450.00
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
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1453	1,500	2453	750	Petition to revive – unintentional	
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8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
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SUBMITTED BY					Complete (if applicable)
Name (Print/Type)	Sumit Bhattacharya	Registration No. (Attorney/Agent)	51,469	Telephone	(408) 975-7500
Signature				Date	March 21, 2006

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First Named Inventor	Thomas D. FLETCHER
Examiner Name	Chat C. DO
Art Unit	2193
Attorney Docket No.	Intel 2207/11270

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Independent Claims		-**	=	X	200.00	=	
Multiple Dependent				X		=	

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1802	900	1802	900	Request for expedited examination of a design application	

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SUBTOTAL (3) ($) 950.00

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Name (Print/Type)	Sumit Bhattacharya	Registration No. (Attorney/Agent)	51,469	Telephone	(408) 975-7500
Signature				Date	March 21, 2006

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Patent

Attorney Docket No.: Intel 2207/11270
Serial No.: 09/956,903
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Thomas D. FLETCHER
SERIAL NO.	:	09/956,903
FILING DATE	:	September 21, 2001
GROUP ART UNIT	:	2193
FOR	:	SYMMETRIC CASCADED DOMINO CARRY GENERATE GATE
EXAMINER	:	Chat C. DO

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APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on November 21, 2005.

1. REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Assignment recorded September 21, 2001, Reel/Frame 012201/0172).

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2. RELATED APPEALS AND INTERFERENCES

There are no related appeals.

3. STATUS OF THE CLAIMS

Claims 1-14, 16-21 and 23-31 are pending in the application. Claims 20-31 are allowed. Claims 1-14 are rejected are rejected under 35 U.S.C. §102(e) as being anticipated by Winters (U.S. 6,292,818). Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. STATUS OF AMENDMENTS

The claims listed on page 1 of the Appendix attached to this Appeal Brief reflect the present status of the claims.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The embodiment of claim 1 generally describes an apparatus comprising a symmetric differential domino carry generate circuit (*see* e.g., page 5 line 5 – Figure 1, 100) having true inputs and compliment inputs which both have a load (*see* e.g., page 8 line 20-22 – Figure 2, 203 and 204), wherein the load for the true inputs is equal to the load for the compliment inputs(*see* e.g., page 5 lines 1-2).

The embodiment of claim 4 generally describes an apparatus comprising a differential domino carry generate circuit (*see* e.g., page 5 line 5 – Figure 1, 100) having a first evaluation block of switches (*see* e.g., page 6 line 4 – Figure 1, 150) and a second evaluation block of

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switches (*see* e.g., page 6 line 5 – Figure 1, 160), wherein the first evaluation block and second evaluation block each have the same number of switches connected in parallel and each have the same number of switches connected in series (*see* e.g., page 4 line 3-5), and wherein the circuit also has a true carry generate output (*see* e.g., page 5 lines 22-23 – Figure 1, 115) and a compliment carry generate output (*see* e.g., page 5 lines 23-24 – Figure 1, 125) which both have an output drive strength, and wherein the output drive strength for said true output is the same as the output drive strength for said compliment output (*see* e.g., page 5 lines 1-2).

The embodiment of claim 10 generally describes an apparatus comprising: a first output to provide a precharge value during a precharge phase (*see* e.g., page 8 lines 18-20 – Figure 2, 202) and a true carry generate value during an evaluation phase (*see* e.g., page 8 lines 22-25, Figure 2, 205); a second output to provide the precharge value during the precharge phase (*see* e.g., page 12 lines 18-20) and the compliment of the true carry generate true during the evaluation phase (*see* e.g., page 10 lines 1-4); a current input (*see* e.g., page 10 lines 5-6); a first evaluation block connected to the current input and the second output and having a plurality of transistors (*see* e.g., page 6 lines 4-7 – Figure 1, 150), wherein a number of said transistors are connected in a parallel relationship and a number of said transistors are connected in a serial relationship (*see* e.g., page 4 line 3-5), wherein the first evaluation block comprises a first transistor with a drain connected to the second output (*see* e.g., page 6 line 25 – Figure 1, 151), a second transistor with a drain connected to the source of the first transistor and a source connected to the current input (*see* e.g., page 6 line 25 – Figure 1, 152), a third transistor with a drain connected to the second output (*see* e.g., page 6 line 25 – Figure 1, 153), a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input (*see* e.g., page 6 line 25 – Figure 1, 154), and a fifth transistor with a drain connected to the

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second output and a source connected to the drain of the fourth transistor (*see* e.g., page 6 line 25 – Figure 1, 155); and a second evaluation block connected to the current input and the first output and having a plurality of transistors (*see* e.g., page 6 line 5 – Figure 1, 160), wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block (*see* e.g., page 4 line 3-5).

The embodiment of claim 20 generally describes an apparatus comprising: a true sum to provide a precharge signal during the precharge phase (*see* e.g., page 8 lines 18-20) and the result of a sum function during the evaluation phase (*see* e.g., page 8 lines 22-25); a compliment sum output to provide the precharge signal during the precharge (*see* e.g., page 12 lines 18-20) and the compliment of the true sum output during the evaluation phase; a current input (*see* e.g., page 10 lines 1-4); a first evaluation block connected to the current input, the true sum output, and the compliment sum output, wherein the first evaluation block has a plurality of transistors (*see* e.g., page 6 lines 4-7 – Figure 1, 150), and wherein a number of said transistors are connected in parallel and a number of said transistors are connected in serial (*see* e.g., page 4 line 3-5), wherein the first transistor has a drain connected to the compliment sum output (*see* e.g., page 6 line 25 – Figure 1, 151), the second transistor has a drain connected to the source of the first transistor and a source connected to the drain of the fifth transistor (*see* e.g., page 6 line 25 – Figure 1, 152), the third transistor has a drain connected to the true sum output (*see* e.g., page 6 line 25 – Figure 1, 153), the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor (*see* e.g., page 6 line 25 – Figure 1, 154), and the fifth transistor has a source connected to the current input; and a second evaluation block connected to the current input and the true sum output and having a plurality of

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transistors (*see* e.g., page 6 line 25 – Figure 1, 155), wherein the second evaluation block (*see* e.g., page 6 line 5 – Figure 1, 160) has the same number of transistors connected in parallel as the first evaluation block and the same number of transistors connected in serial as the first evaluation block(*see* e.g., page 4 line 3-5).

The embodiment of claim 25 generally describes a method comprising: receiving at a first evaluation block three true input values; receiving at a second evaluation block three compliment input values, wherein the compliment input values are the compliment of the true input values (*see* e.g., page 8 line 20-22 – Figure 2, 203 and 204); processing the compliment input values at the second evaluation block to provide a carry generate value at a first output (*see* e.g., page 6 line 5 – Figure 1, 160) by selecting one of a plurality of stacks of transistors in the second evaluation block, wherein each of said stacks of transistors connects a current input to the first output (*see* e.g., page 10 line 13-15); and processing the true input values at the first evaluation block to provide the compliment of the carry generate value at a second output by selecting one of a plurality of stacks of transistors in the first evaluation block(*see* e.g., page 8 line 2- page 9, - Figure 2, 206 & 208), wherein each of said stacks of transistors connects said current input to the second output, and wherein the first evaluation block and second evaluation block have the same number of stacks of transistors (*see* e.g., page 4 line 3-5).

FIG. 1 is a block diagram of a symmetric differential domino carry generate circuit according to an embodiment of the present invention. FIG. 1 shows differential domino carry generate circuit 100 that may provide a carry generate bit (115) as an output based on two input data bits (*a* 111 and *b* 112) and a carry input bit (113). Carry generate circuit 100 has a clock input 101, an input for an data bit value "*a*" 111, an input for an data bit value "*b*" 112, and a carry input bit 113. These inputs are the "true" inputs to the circuit. As would be appreciated by

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a person of skill in the art, an input "value" that is received by carry generate circuit 100, or output by carry generate circuit 100, is a voltage range that represents a logical value. The inputs at *a* 111 and *b* 112 each may represent, for example, a single bit of two binary numbers being added by an adder of which carry generate circuit 100 may be a part. In this embodiment, and as would be appreciated by a person of skill in the art, the carry input 113 may be the carry from the previous logic stage.

In the embodiment shown in FIG. 1, differential domino carry generate circuit 100 has a transistor 171, two precharge transistors (first precharge transistor 141 and second precharge transistor 142), a keeper 180, a first evaluation block 150, and a second evaluation block 160. In this embodiment, transistor 171 has a source terminal ("source") connected to ground, a drain terminal ("drain") connected to first evaluation block 150 and second evaluation block 160, and a gate connected to clock input 101. As used herein, two circuit elements are connected if they are directly connected or indirectly connected to create an electrical path (i.e., as through an inter-connection line). Transistor 171 may be referred to as a "footer" transistor because it is at the bottom of the evaluation blocks. In this embodiment, footer transistor 171 is an NMOS transistor. In other embodiments, the circuit may not have a clocked transistor at the bottom of the evaluation stacks. In an embodiment, clock 101 is also connected to the gates of first precharge transistor 141 and second precharge transistor 142. In an embodiment, first precharge transistor 141 and second precharge transistor 142 are PMOS transistors, and the sources of first precharge transistor 141 and second precharge transistor 142 are each connected to Vcc. The drain of first precharge transistor 141 may be connected to compliment carry generate 125, and the drain of second precharge transistor 142 may be connected to carry generate 115. In this embodiment first precharge transistor 141 and second precharge transistor 142 determine outputs

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of carry generate circuit 100 during the precharge phase, and footer transistor 171 enables the determination of the outputs of carry generate circuit 100 by the evaluation blocks during the evaluation phase.

FIG. 2 is a flow diagram of a method of processing data in a symmetric carry generate circuit according to an embodiment of the present invention. The method shown in FIG. 2 will be discussed with reference to the carry generate circuit 100 shown in FIG. 1, but of course this method could also be used with other embodiments. A precharge phase of a clock may be first received by carry generate circuit 100 at clock input 101 (201). During the precharge phase, a precharge output value (e.g., a logical high) may be continuously provided at first and second outputs of the carry generate circuit such as at carry generate output 115 and compliment carry generate output 125 (202). As shown in FIG. 2, true and compliment input values may also be received during the precharge phase at inputs 111-113 and 121-123 (203 and 204). When the clock cycles to the evaluation phase (205), the precharge transistors may stop providing the precharge value at the outputs, and the footer transistor 171 may provide a current to transistors in first evaluation block 150 and second evaluation block 160. As shown in FIG. 2, the first evaluation block processes the true input values (206) and provides a compliment carry generate value at a first output based on these true input values (208). That is, the first evaluation block may provide an output at compliment carry generate 125 based on the true input values. At approximately the same time, the second evaluation block processes the compliment input values (207) and provides a carry generate value at a second output based on these compliment input values (209). That is, the second evaluation block may provide an output at carry generate 115 based on the compliment input values. Carry generate circuit 100 may maintain the carry

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generate and compliment carry generate values at the respective outputs (210) until the clock cycles back to the precharge phase, which causes the process to be repeated (201).

FIG. 3 is a block diagram of a symmetric differential domino intermediate group carry generate circuit 300 according to an embodiment of the present invention.

FIG. 4 is a block diagram of a symmetric differential domino final group carry generate circuit 400 according to an embodiment of the present invention.

FIG. 5 is a block diagram of a symmetric differential domino carry generate circuit according to another embodiment of the present invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-9 are rejected are rejected under 35 U.S.C. §102(e) as being anticipated by Winters (U.S. 6,292,818).

B. Claims 10-14 are rejected are rejected under 35 U.S.C. §102(e) as being anticipated by Winters (U.S. 6,292,818).

7. ARGUMENT

First, Applicant would like to gratefully acknowledge the Examiner's allowance of claims 20-31. *See Advisory Action.* Applicant further gratefully acknowledges the Office Action's indication that claims 16-19 contain allowable subject matter.

A. Claims 1-9 are not anticipated under 35 U.S.C. §102(e) Winters.

Applicant submits that the cited prior art does not teach, suggest, or disclose "[a]n apparatus comprising a symmetric differential domino carry generate circuit having true inputs

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and compliment inputs which both have a load, wherein the load for the true inputs is equal to the load for the compliment inputs" (e.g., as described in claim 1).

In its rejection, the Examiner cites generally to Figure 6 as disclosing the relevant limitations, with no further specific citation. See Office Action dated 5/19/2005, page 3, line 5. In the Response to Arguments section of this Office Action, the Examiner states that the cited reference clearly discloses in Figure 6 the true inputs (e.g. A1H, B1H and C1H) (the "H set") and the complement inputs (e.g., A1L, B1L and C1L) (the "L set"), further claiming they are complements to each other having equal load. Applicant disagrees.

Winters is silent as to the relationship between the two input sets "H" and L." Figure 6 is described in the three paragraphs of Winters, spanning column 5, line 35 to column 6 line 10. The first paragraph describes a schematic diagram of the propagate/generate logic block shown in Figure 3. The second paragraph describes the dynamic logic gate comprised of circuits 21A and 21B used to generate and propagate static outputs. It further states that: "Nodes identified in Fig. 6 with identical reference numbers are coupled together". See column 5, line 52. However, there is no further description of the nodes, and there is no description in the specification whatsoever that any inputs are complimentary as described in the embodiment of claim 1. The last paragraph describes the manner in which the precharged nodes are charged by PMOS FETs in response to a clock signal that is high/low. Applicant maintains however, there is no description in the specification that any inputs, including the alleged the "H" set and the "L" set, are complimentary (or that they have an equal load) as described in the embodiment of claim 1. Assuming that the "H" set of inputs is a "high" set and the "L" set of inputs is a "low" set, *arguendo*, Applicant submits the generic disclosure of a "high" and "low" signal set is insufficient to disclose *compliment inputs* which both have a load, wherein the load for the true

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inputs *is equal* to the load for the compliment inputs as specifically recited in the embodiment of claim 1

Therefore, Applicant submits that the Examiner's claim that these two input sets are compliments to each other is completely unsupported by the reference. Applicant notes that in the initial rejection, despite the Office Action's claims, there was no specific citation to any section of Winters, but rather a generic reference to Figure 6 as a whole. In the recent Office Action and its Response, again there is no reference to a specific place in Winters as disclosing the relevant limitations, but a general citation supplemented by an unsupported assertion.

The assertions in the Advisory Action are inadequate for similar reasons. As shown above, the Winters reference neither describes "H" set and the "L" set as compliments, nor as having an equal load. Nevertheless, the Examiner asserts "...the load of true is equal to the load of their complement because they are complement to each other". These unsupported and conveniently circular assertions are insufficient to support a proper §102(e) rejection *without further support* from the Winters reference itself. Moreover, in addressing the Examiner's other remarks, that these must have a "input load" or have the signal strengths to identify or drive other circuits/components *does not mean they are* compliment inputs which both have a load, wherein the load for the true inputs is equal to the load for the compliment inputs as described in the embodiment of claim 1.

In light of the arguments made above, and the need for each rejection to be taught, suggested or disclosed by the reference, Applicant submits that the Winters reference is inadequate to support a proper 35 U.S.C. 102(e) reference, and the rejection should be withdrawn. Independent claim 4 contains similar allowable limitations. Claims 2-3 and 5-9 are allowable for depending from allowable base claims.

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B. Claims 10-14 are allowable over Winters and the art of record

Next, Applicant submits the cited reference does not teach, suggest, or disclose at least "[a]n apparatus comprising...a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor..." (e.g., as described in claim 10).

In the response section of the most recent Office Action (see Page 8, paragraph b), the Examiner claims that Figure 6 discloses first, second, third, fourth and fifth transistors wherein a fourth transistor with a drain connected to the source of the third transistor (e.g., transistor on the left for receiving A1L) and a fifth transistor (e.g., transistor for receiving A1H) with a drain connected to the second output (e.g., either 25/26 as EVAL) and a source connected to the drain of the fourth transistor. Applicant disagrees.

As described in the summary of the description of Figure 6 detailed above, there is no mention of any transistors connected to drains. Moreover, Applicant notes that while the Examiner cites elements A1H, B1H... etc. as allegedly disclosing transistors, there is no specific citation to the drains corresponding to the transistors as specifically recited in the embodiment of claim 10. The Office Action cites the A1H, B1H ...etc., which as asserted above, are not described in the specification at all as being in conjunction with a drain. In fact, the elements A1H, B1H, ... etc., are not transistors, but rather merely shown to be *inputs supplied to the gates of the transistors* shown in Figure 6. Moreover, cited elements 25/26 (also cited in the Advisory Action) are PMOS FETs (see column 5, line 58), which also are not accompanied by any descriptions of associated drains. Lastly, an examination of Figure 6 of Winters illustrates the

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lack of any associated drains connected with any of the elements (or more particularly, to the appropriate sources) of Figure 6, as specifically described in the embodiment of claim 10.

In order to support a proper 35 U.S.C. 102(e) rejection, each and every limitation of the claim must be found in the cited reference. However, since the Winters does not teach, disclose or even suggest at least the use of transistors in association with drains at all, the rejection is improper and should be withdrawn. Dependent claims 11-14 are allowable as depending from an allowable base claim.

Appellants therefore respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1-14 and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge the appeal brief fee of **$500.00** and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

Date: March 21, 2006

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Advisory Action dated December 15, 2005

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APPENDIX

(Brief of Appellant Thomas D. Fletcher
U.S. Patent Application Serial No. 09/956,903)

8. CLAIMS ON APPEAL

1. (Previously presented) An apparatus comprising a symmetric differential domino carry generate circuit having true inputs and compliment inputs which both have a load, wherein the load for the true inputs is equal to the load for the compliment inputs.

2. (Previously presented) The apparatus of claim 1, wherein the circuit also has a true carry generate output and a compliment carry generate output which both have an output drive strength, and wherein the output drive strength for said true output is the same as the output drive strength for said compliment output.

3. (Previously presented) The apparatus of claim 1, wherein the circuit further comprises:

a first evaluation block having a plurality of transistors, wherein a number *p* of said transistors are connected in a parallel relationship and a number *s* of said transistors are connected in a serial relationship; and

a second evaluation block having a plurality of transistors, wherein in the second evaluation block *p* transistors are connected in a parallel relationship and *s* transistors are connected in a serial relationship.

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4. (Previously presented) An apparatus comprising a differential domino carry generate circuit having a first evaluation block of switches and a second evaluation block of switches, wherein the first evaluation block and second evaluation block each have the same number of switches connected in parallel and each have the same number of switches connected in series, and wherein the circuit also has a true carry generate output and a compliment carry generate output which both have an output drive strength, and wherein the output drive strength for said true output is the same as the output drive strength for said compliment output.

5. (Original) The apparatus of claim 4, wherein the switches in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors.

6. (Original) The apparatus of claim 5, wherein corresponding transistors in the first evaluation block and second evaluation block are the same size.

7. (Original) The apparatus of claim 4, wherein the apparatus further comprises cross-coupled P-channel metal-oxide semiconductor (PMOS) keeper transistors.

8. (Original) The apparatus of claim 4, wherein the differential domino carry generate circuit is a first stage in a carry look-ahead adder.

9. (Original) The apparatus of claim 4, wherein the differential domino carry generate circuit is a group generate gate.

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10. (Previously presented) An apparatus comprising:

a first output to provide a precharge value during a precharge phase and a true carry generate value during an evaluation phase;

a second output to provide the precharge value during the precharge phase and the compliment of the true carry generate true during the evaluation phase;

a current input;

a first evaluation block connected to the current input and the second output and having a plurality of transistors, wherein a number of said transistors are connected in a parallel relationship and a number of said transistors are connected in a serial relationship, wherein the first evaluation block comprises a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor; and

a second evaluation block connected to the current input and the first output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block.

11. (Original) The apparatus of claim 10, wherein the output drive strength for the first output is the same as the output drive strength for the second output.

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12. (Previously presented) The apparatus of claim 10, wherein the circuit further comprises a clock input to receive a clock having precharge and evaluation phases.

13. (Previously presented) The apparatus of claim 12, wherein the current input is a transistor having a source node connected to ground and a gate connected to the clock input.

14. (Original) The apparatus of claim 13, wherein the gate of each transistor in the first evaluation block is connected to one of a set of true inputs and the gate of each of the transistors in the second evaluation block is connected to one of a set of compliment inputs, and wherein the load for the true inputs is the same as the load for the compliment inputs.

15. (Cancelled)

16. (Previously presented) The apparatus of claim 12, wherein the gates of the first transistor and third transistor are connected to a first of the true inputs, the gates of the second transistor and fifth transistor are connected to a second of the true inputs, and the gate of the fourth transistor is connected to a third of the true inputs.

17. (Original) The apparatus of claim 16, wherein the precharge block comprises a first precharge transistor connected to a second current input and a second precharge transistor connected to a third current input, and wherein the first and second precharge transistors each have a gate connected to the clock.

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18. (Original) The apparatus of claim 17, wherein the apparatus further comprises a keeper connected to each of the first output, second output, first evaluation block, and second evaluation block.

19. (Original) The apparatus of claim 18, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors, wherein first and second precharge transistor are P-channel metal-oxide semiconductor (PMOS) transistors, and wherein the keeper comprises two PMOS transistors.

20. (Previously presented) An apparatus comprising:

a true sum to provide a precharge signal during the precharge phase and the result of a sum function during the evaluation phase;

a compliment sum output to provide the precharge signal during the precharge phase and the compliment of the true sum output during the evaluation phase;

a current input;

a first evaluation block connected to the current input, the true sum output, and the compliment sum output, wherein the first evaluation block has a plurality of transistors, and wherein a number of said transistors are connected in parallel and a number of said transistors are connected in serial, wherein the first transistor has a drain connected to the compliment sum output, the second transistor has a drain connected to the source of the first transistor and a

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source connected to the drain of the fifth transistor, the third transistor has a drain connected to the true sum output, the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor, and the fifth transistor has a source connected to the current input; and

a second evaluation block connected to the current input and the true sum output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in parallel as the first evaluation block and the same number of transistors connected in serial as the first evaluation block.

21. (Original) The apparatus of claim 20, wherein the output drive strength for the true sum output is the same as the output drive strength for the compliment sum output.

22. (Cancelled)

23. (Previously presented) The apparatus of claim 20, wherein the gate of the first transistor is connected to an exclusive-OR input, the gate of the second transistor is connected to a first generate input, the gate of the third transistor is connected to a compliment exclusive-OR input, the gate of the fourth transistor is connected to a second generate input, and the gate of the fifth transistor is connected to a propagate input.

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24. (Original) The apparatus of claim 20, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors.

25. (Previously presented) A method comprising:

receiving at a first evaluation block three true input values;

receiving at a second evaluation block three compliment input values, wherein the compliment input values are the compliment of the true input values;

processing the compliment input values at the second evaluation block to provide a carry generate value at a first output by selecting one of a plurality of stacks of transistors in the second evaluation block, wherein each of said stacks of transistors connects a current input to the first output; and

processing the true input values at the first evaluation block to provide the compliment of the carry generate value at a second output by selecting one of a plurality of stacks of transistors in the first evaluation block, wherein each of said stacks of transistors connects said current input to the second output, and wherein the first evaluation block and second evaluation block have the same number of stacks of transistors.

26. (Original) The method of claim 25, wherein the first evaluation block and second evaluation block have corresponding stacks that have the same number of transistors.

27. (Previously presented) The method of claim 25, wherein the method further comprises:

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receiving a clock having a precharge phase and an evaluation phase;

providing precharge values at the first output and at the second output during said precharge phase; and

providing the compliment carry generate value at the first output and the carry generate value at the second output during the evaluation phase.

28. (Original) The method of claim 27, wherein the method further comprises preventing current from passing through the current input during the precharge phase and enabling current to pass through the current input during the evaluation phase.

29. (Original) The method of claim 28, wherein the method further comprises:

providing the output from the first evaluation block to a keeper;

providing the output from the second evaluation block to a keeper; and

providing the carry generate true output and carry generate compliment output during the evaluation phase based upon output from the first evaluation block, second evaluation block, and the keeper.

30. (Original) The method of claim 25, wherein the inputs received and outputs provided are symmetrical.

31. (Previously presented) The method of claim 25, wherein the first evaluation block has three stacks of transistors, and wherein the second evaluation block has three stacks of transistors.

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9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

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10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.

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